WHAT IS CLAIMED:

1. A pipelined processor comprising:

a first pipeline stage including:

a plurality of instruction memories, and

a program counter configured to read instructions from the plurality of instruction memories; and

a second pipeline stage including:

a priority encoder configured to select one of the instructions based on evaluation results generated from the instructions read from the instruction memories, and

an execution unit configured to receive the selected one of the instructions and to perform operations indicated by the selected instruction.

2. The pipelined processor of claim 1, wherein the operation performed by the execution unit relates to processing of packet header information.

3. The pipelined processor of claim 1, further comprising:

a packet header buffer connected to the priority encoder and the execution unit.

4. The pipelined processor of claim 1, wherein the instructions are read from a memory address equal to the value of the program counter.

5. The pipelined processing processor of claim 1, wherein the second pipeline stage further comprises:

an evaluation component corresponding to each of the instruction memories, the evaluation components generating the evaluation results based on each of the instructions read from the instruction memories.

6. The pipelined processor of claim 5, wherein the evaluation components generate the evaluation results based on a logical operation dictated by the instructions.

7. The pipelined processor of claim 1, further comprising:

a branch prediction component configured to generate a predicted program counter value based on instructions read from one of the instruction memories, wherein

the execution unit generates a true program counter value based on the selected instruction and generates an indication of whether the predicted program counter value is accurate.

8. The pipelined processor of claim 1, wherein the second pipeline stage further comprises:

a multiplexer configured to receive the read instructions and to forward the selected one of the instructions to the execution unit based on a signal from the priority encoder.

9. The pipelined processor of claim 1, further comprising:

a plurality of memory elements implemented as an interface between the first and second pipeline stages.

10. A network device comprising:

a physical interface configured to receive packets from and transmit packets to a network; and

a processing unit configured to store the received packets and to examine header information of the packets, the processing unit including a pipelined packet processing engine that comprises:

a first pipeline stage configured to read a plurality of packet processing instructions from instruction memory, and

a second pipeline stage configured to select one of the instructions for execution.

11. The network device of claim 10, wherein the network device is a router.

12. The network device of claim 10, wherein the first pipeline stage comprises:

a program counter configured to store a program address value used to read the packet processing instructions from the instruction memories.

13. The network device of claim 10, wherein the second pipeline stage comprises:

a priority encoder configured to select the one of the packet processing instructions based on evaluation results generated from the packet processing instructions read from the instruction memories, and

an execution unit configured to receive the selected one of the packet processing instructions and to perform operations indicated by the selected packet processing instruction.

14. The network device of claim 13, wherein the instructions read from the instruction memories are read from a memory address equal to the value of the program counter.

15. The network device of claim 13, wherein the second pipeline stage further comprises:

an evaluation component corresponding to each of the instruction memories, the evaluation components generating the evaluation results based on each of the instructions read from the instruction memories.

16. The network device of claim 15, further comprising:

a packet header buffer connected to evaluation component.

17. The network device of claim 15, wherein the evaluation components generate the evaluation results based on a logical operation dictated by the packet processing instructions.

18. The network device of claim 10, further comprising:

a branch prediction component configured to generate a predicted program counter value based on packet processing instructions read from one of the instruction memories, wherein

an execution unit generates a true program counter value based on the selected packet processing instruction and generates an indication of whether the predicted program counter value is accurate.

19. The network device of claim 10, wherein the second pipeline stage further comprises:

a multiplexer configured to receive the read packet processing instructions and to forward the selected one of the packet processing instructions to an execution unit based on a signal from the priority encoder.

20. The network device of claim 10, further comprising:

a plurality of timing buffers implemented as an interface between the first and second pipeline stages.

21. A method for processing a packet to determine control information for the packet, the method comprising:

reading a plurality of instructions;

generating a predicted address based on a predetermined one of the plurality of instructions;

evaluating the read instructions;

selecting one of the read instructions based on the evaluations; and

performing operations related to determining the control information for the packet based on the selected instruction, the operations including generating a true next address for reading instructions.

22. The method of claim 21, wherein evaluating the read instructions is performed based on a field in the instructions that specifies a logical operation that is to be performed.

23. The method of claim 21, wherein the method is performed in two pipelined stages.

24. The method of claim 21, wherein the selecting of one of the read instructions is performed as a priority selection based on a read instruction that evaluates to a logic true value.

25. The method of claim 21, wherein the operation includes an extract instruction that is used to extract designated information from the packet into a memory.

26. The method of claim 21, wherein the operation includes a write instruction used to write information contained in a field of the write instruction to a memory.

27. A pipelined processing device comprising:

means for reading a plurality of packet processing instructions from instruction memory; and

means for selecting one of the read instructions for execution based on a priority encoding of evaluation results related to each of the read instructions.

28. The pipelined processing device of claim 27, wherein the means for reading and the means for selecting are implemented as first and second stages of the pipeline, respectively.

29. The pipelined processing device of claim 27, further comprising:

means for storing a value that designates an address to the instruction memory.

30. The pipelined processing device of claim 29, further comprising:

means for generating a predicted next value to store in the means for storing; and

means for generating a true next value to store in the means for storing.